REMARKS

Initially, Applicants express appreciation to the Examiner for the detailed Official Action provided.

Upon entry of the present paper, claims 13-26 (*i.e.*, all pending claims) will have been amended. The herein contained amendments should not be considered an acquiescence in the propriety of the outstanding rejections. Rather, the claims have been amended to eliminate possible means-plus-function claim language and to clarify the features recited therein. Furthermore, it is submitted that no prohibited new matter has been introduced by the abovementioned amendments. Specifically, the amendments to claims 13 and 23 are submitted to be supported at least by page 9, lines 9-21 of the present application as filed on October 11, 2006 (¶[0059] of corresponding U.S. Appl. Pub. No. 2007/0208919). Thus, claims 13-26 are pending in the present application with claims 13 and 23 being in independent form.

Applicants address the pending rejections provided within the outstanding Official Action below and respectfully request reconsideration and withdrawal thereof together with an indication of the allowability of claims 13-26 (*i.e.*, all pending claims) in the next Official communication. Such action is respectfully requested and is now believed to be appropriate for at least the reasons provided below.

35 U.S.C. § 103 Claim Rejections

In the outstanding Official Action, claims 13, 14, and 23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Pat. No. 6,075,899 to Yoshioka et al.

(hereinafter "YOSHIOKA") in view of U.S. Appl. Pub. No. 2003/0113026 to Srinivasan et al. (hereinafter "SRINIVASAN").

Initially, Applicants again note that, upon entry of the present paper and without acquiescing in the propriety of the above-mentioned rejection, independent claims 13 and 23 (*i.e.*, all pending independent claims) will have been amended to clarify the features recited therein. In this regard, Applicants traverse the rejection.

Independent claims 13 and 23 recite, respectively, an information processing device and a data access method. According to the features of independent claim 13 as a non-limiting and exemplary embodiment of the independent claims, a DRAM stores image data in a rectangular area of M pixels × N lines. The DRAM has a burst mode which burst-transfers data of successive column addresses. A data processor issues an access request, and, in response to the access request, an address converter converts access addresses of the image data such that a column address of data at a $(K+m)^{th}$ column of an L^{th} line and a column address of data at a K^{th} column of an $(L+n)^{th}$ line become successive, wherein $n = 2n'$ and K, m, L, n, and n' are positive integers. In other words, column addresses of every other line (or every fourth line, sixth line, etc.) become successive.

According to amended independent claim 13, the DRAM burst-transfers the data at the $(K+m)^{th}$ column of the L^{th} line and the data at the K^{th} column of the $(L+n)^{th}$ line in the burst mode by successively accessing the column address of the data at the $(K+m)^{th}$ column of the L^{th} line and the column address of the data at the K^{th} column of the $(L+n)^{th}$ line. According to a non-limiting and advantageous effect of such a feature, when image data is estimated by skipping a line of the image data, such as in motion compensation or

motion estimation processing for an interlaced video, the unnecessary transfer load is reduced and the effective bandwidth is improved in a short burst-length access such as a rectangular access.

Applicants respectfully submit that YOSHIOKA and SRINIVASAN, whether considered alone or together in any proper combination thereof, fail to disclose at least the features of independent claims 13 and 23, as generally recited in the claimed combinations, of: converting access addresses so that a column address of data at a $(K+m)^{th}$ column of an L^{th} line and a column address of data at a K^{th} column of an $(L+n)^{th}$ line become successive, wherein n=2n' and K, m, L, n, and n' are positive integers; and burst-transferring the data at the $(K+m)^{th}$ column of the L^{th} line and the data at the K^{th} column of the $(L+n)^{th}$ line in the burst mode by successively accessing the column address of the data at the $(K+m)^{th}$ column of the L^{th} line and the column address of the data at the K^{th} column of the $(L+n)^{th}$ line.

In Applicants' previous Response filed on November 19, 2009, Applicants' generally submitted that YOSHIOKA fails to disclose at least the feature of converting access addresses so that a column address of data at a $(K+m)^{th}$ column of an L^{th} line and a column address of data at a K^{th} column of an $(L+n)^{th}$ line become successive, wherein n=2n' and K, m, L, n, and n' are positive integers. In the outstanding Official Action, the Examiner appears to generally acknowledge that YOSHIOKA fails to disclose such a feature (*see* page 3, lines 15-16 of the outstanding Official Action).

Furthermore, with respect to the feature of burst transferring the data at the $(K+m)^{th}$ column of the L^{th} line and the data at the K^{th} column of the $(L+n)^{th}$ line in the burst mode by successively accessing the column addresses of the data, Applicants

submit that YOSHIOKA merely discloses burst transferring data on a single page (*i.e.*, data within a single row) (*see, e.g.*, YOSHIOKA, col. 12, lines 60-66 and col. 15, lines 27-29). Applicants respectfully submit that such disclosure of YOSHIOKA fails to disclose or render obvious the above-mentioned feature of independent claims 13 and 23 of burst transferring data at a $(K+m)^{th}$ column of an L^{th} line and a column address of data at a K^{th} column of an $(L+n)^{th}$ line by successively accessing the column addresses of the data (*i.e.*, burst transferring data at every other line (or every fourth line, sixth line, etc.)).

Applicants further submit that SRINIVASAN similarly fails to disclose or render obvious the above-mentioned features of independent claims 13 and 23 of the present application as recited in the claimed combinations. To the contrary, SRINIVASAN discloses a video compression technique including a row-prediction method for macroblock coding (SRINIVASAN, ¶[0005]). According to SRINIVASAN, each macroblock row includes a bit, or flag, that indicates whether all of the macroblocks in the corresponding macroblock row are to be skipped (*i.e.*, whether the corresponding macroblock row includes any macroblocks which are to be encoded/decoded) (SRINIVASAN, Figure 15 and ¶[0131]). If the bit indicates that all of the macroblocks in the corresponding macroblock row are not to be skipped (*i.e.*, the corresponding macroblock row includes macroblocks which are to be encoded/decoded), then a bit field equal in length to the number of macroblocks in the corresponding macroblock row indicates which of the macroblocks are to be encoded/decoded (*see* SRINIVASAN, Figure 15 and ¶[0132]).

In the outstanding Official Action, it appears that the Examiner asserts that SRINIVASAN may be reasonably interpreted to disclose that every other macroblock

row could be entirely skipped, and thus, that SRINIVASAN discloses the above-mentioned feature of the independent claims of the present application, as recited in the claimed combinations, of converting access addresses so that a column address of data at a $(K+m)^{th}$ column of an L^{th} line and a column address of data at a K^{th} column of an $(L+n)^{th}$ line become successive. Applicants respectfully disagree and submit that, even if SRINIVASAN is interpreted to disclose that every other macroblock row is entirely skipped, SRINIVASAN fails to disclose that the access addresses of the macroblocks are converted.

To the contrary, SRINIVASAN merely appears to disclose that the necessary macroblocks within a macroblock row are indicated within a bit field. Thereafter, SRINIVASAN discloses that only the necessary macroblocks are encoded/decoded based upon reading the bit field. In other words, even if SRINIVASAN is interpreted to disclose that a macroblock at a $(K+m)^{th}$ column of an L^{th} macroblock row and a macroblock at a K^{th} column of an $(L+n)^{th}$ macroblock row are indicated, in the corresponding bit fields, to be necessary for encoding/decoding, Applicants respectfully submit that such disclosure cannot be reasonably interpreted to disclose that the access addresses of the macroblocks are converted so that the column addresses become successive. That is, Applicants respectfully submit that indicating necessary macroblocks in a bit field, as disclosed by SRINIVASAN, cannot be reasonably interpreted to disclose or render obvious the feature of independent claims 13 and 23 of the present application of converting access addresses so that a column address of data at a $(K+m)^{th}$ column of an L^{th} line and a column address of data at a K^{th} column of an $(L+n)^{th}$ line become successive, wherein $n=2n'$ and K, m, L, n, and n' are positive integers.

Furthermore, additionally to, and independently of, the above, Applicants further submit that SRINIVASAN fails to disclose or render obvious the feature of independent claims 13 and 23 of the present application, as recited in the claimed combinations, of burst-transferring the data at the $(K+m)^{th}$ column of the L^{th} line and the data at the K^{th} column of the $(L+n)^{th}$ line in the burst mode by successively accessing the column address of the data at the $(K+m)^{th}$ column of the L^{th} line and the column address of the data at the K^{th} column of the $(L+n)^{th}$ line. In this regard, SRINIVASAN does not even appear to disclose burst-transferring data. Rather, SRINIVASAN merely appears to disclose reading a flag of a first macroblock row to determine whether any macroblocks within the first macroblock row are to be encoded/decoded, reading a bit field to determine which macroblocks within the first macroblock row are to be encoded/decoded, reading a flag of a second macroblock row to determine whether any macroblocks within the first macroblock row are to be encoded/decoded, reading a bit field to determine which macroblocks within the second macroblock row are to be encoded/decoded, etc. (*see* SRINIVASAN, Figure 15). In view of the above, Applicants respectfully submit that SRINIVASAN cannot be reasonably interpreted to disclose that macroblocks of different macroblock rows are read via a burst mode, and thus, that SRINIVASAN cannot be reasonably interpreted to disclose or render obvious the above-mentioned feature of independent claims 13 and 23 of the present application as recited in the claimed combinations.

Accordingly, at least in view of the above, Applicants respectfully submit that the combination of YOSHIOKA and SRINIVASAN fails to render obvious amended independent claims 13 and 23. Thus, Applicants respectfully request that the 35 U.S.C. §

103 rejection of independent claims 13 and 23 is withdrawn and that these claims are indicated to be allowable in the next Official communication.

With respect to dependent claim 14, Applicants submit that this claim is directly dependent from independent claim 13, which is allowable for at least the reasons discussed *supra*. Thus, it is submitted that this dependent claim is also allowable at least for the reasons discussed *supra*. Furthermore, this dependent claim recites additional features which further define the present invention over the references of record.

35 U.S.C. § 103 Rejection of Dependent Claims 15-22 and 24-26

In the outstanding Official Action, claim 15 was rejected under 35 U.S.C. § 103(a) as being unpatentable over YOSHIOKA in view of SRINIVASAN, and further in view of U.S. Pat. No. 6,745,320 to Mitsuishi (hereinafter "MITSUISHI"). Additionally, claims 16-22 and 24-26 were rejected under 35 U.S.C. § 103(a) as being unpatentable over YOSHIOKA in view of SRINIVASAN, in view of MITSUISHI, and further in view of U.S. Pat. No. 6,807,311 to Callway et al. (hereinafter "CALLWAY"). Applicants respectfully traverse these rejections.

Applicants initially note that each of dependent claims 15-22 and 24-26 are directly or indirectly dependent from independent claim 13, which is submitted to be allowable for at least for the reasons discussed *supra*. In this regard, Applicants submit that MITSUISHI and CALLWAY fail to cure the deficiencies of YOSHIOKA and SRINIVASAN, either singularly or in the combination set forth in the outstanding Official Action. To the contrary, MITSUISHI is merely asserted to disclose a general purpose processor with registers available for high speed processing, while CALLWAY merely appears to disclose data compression as opposed to data estimation. Thus, it is

submitted that the combinations of the references set forth in the outstanding Official Action fail to result in Applicants' invention, as defined by independent claims 13 and 23. Accordingly, the dependent claims are submitted to also be allowable for at least the reasons discussed *supra*. Furthermore, the dependent claims recite additional features which further define the present invention over the references of record.

At least in view of the above, Applicants respectfully submit that each and every pending claim of the present application (*i.e.*, claims 13-26) meets the requirements for patentability. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejections and to indicate the allowance of each and every pending claim in the present application.

CONCLUSION

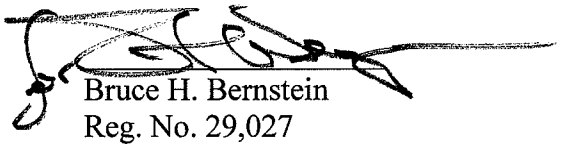
In view of the fact that none of the art of record, whether considered alone, or in any proper combination thereof, discloses or renders obvious the present invention, and in further view of the above remarks, reconsideration of the Examiner's action and allowance of the present application are respectfully requested and are believed to be appropriate.

Applicants note that the amendments to the claims are to be considered merely clarifying amendments that are cosmetic in nature, and are not intended to narrow the scope of the claims. Accordingly, this amendment should not be considered a decision by Applicants to narrow the claims in any way.

Should the Commissioner determine that an extension of time is required in order to render this response timely and/or complete, a formal request for an extension of time, under 37 C.F.R. §1.136(a), is herewith made in an amount equal to the time period required to render this response timely and/or complete. The Commissioner is authorized to charge any required extension of time fee under 37 C.F.R. §1.17 to Deposit Account No. 19-0089.

If there should be any questions concerning this application, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,
Takaharu TANAKA et al.



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